OFFICIAL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
Garg *et al.*	Art Unit: 2783
Appl. No. 09/188,708	Examiner: *To Be Assigned*
Filed: November 10, 1998	Atty. Docket: SP018.C4
For: **RISC Microprocessor Architecture Implementing Multiple Typed Register Sets**	Attention: **Box Non-Fee Amendment**

Preliminary Amendment

RECEIVED
SEP 16 1999
GROUP 2700

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination of the above-captioned application and calculation of a filing fee, please enter the following Amendment.

In the Claims:

Please cancel claim 1.

Please add the following claims 31-43:

31. A processor, comprising:

an execution unit that performs at least one operation according to an instruction;

a first register set including a plurality of first registers each for holding integer data; and

a second register set including a plurality of second registers each for holding said integer data and for holding floating point data,

wherein said instruction specific which of said first and second register sets is to be accessed, and wherein said execution unit accesses said first register set or said second register set as